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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,965	06/20/2001	Hirofumi Honda	05721.0025	4448

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EXAMINER	
AMINI, JAVID A	

ART UNIT	PAPER NUMBER
2672	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,965	HONDA ET AL.	
	Examiner	Art Unit	
	Javid A Amini	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Feb. 10, 2004 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabata et al. (hereinafter referred as a Kawabata-257, U.S. 5,748,257), and Tanaka et al. (hereinafter referred as a Tanaka), and further in view of Izawa et el., U.s. 5,296,941 (hereinafter referred as an Izawa).

1. Claim 1.

"A luminance level compensating apparatus comprising: a first masking device for passing only a luminance signal corresponding to a pixel in a first detection range in the

vertical direction of an image which is indicated by an input luminance signal; *examiner's note: masking devices can limit the illuminated area to a region equal to or smaller than the portion of the image. Kawabata-257 in col. 3, lines 12-16 teaches an area is designated so that picture information necessary for compensating picture quality can be detected. Horizontal and vertical positions, which can be detected over the entire screen, are designated in the picture area signal output circuit1 see fig. 7. Hence, according to the above definition of the masking device circuit1 in fig. 7 contains first and second masking devices. In figs. 6 and 8 illustrate the obviousness of two different pictures p1 and p2. However the quantity of light (luminance/brightness/intensity) is corresponding to a pixel and nothing else. That specifies in the following claim language:* a second masking device for passing only a luminance signal corresponding to a pixel in a second detection range in the vertical direction of the image which is indicated by said input luminance signal, wherein the first detection range corresponds to a first predetermined image area and the second detection range corresponds to a second predetermined area, which is not equal to the first predetermined area; *Examiner reply to the following claim language is: Kawabata-257 does not explicitly specify storing a first frequency for each luminance, however Tanaka illustrates in fig. 5 item 24 that stores the peak value of the luminance signal. And also Kawabata-257 illustrates in figs. 10 and 11 the histograms of luminance signal for the two images (p1 and p2). The step of predetermined period is obvious because in figs. 10 and 11 illustrates the number of sampled signals, which involves in predetermined period.* A first histogram memory device for detecting and storing a first frequency for each luminance level of the luminance signal output from said first

masking device for each predetermined period; a second histogram memory device for detecting and storing a second frequency for each luminance level of the luminance signal output from said second masking device for each predetermined period; Examiner's *reply for the following claim language is: a frequency data mixing device for generating mixed frequency data based on each of the first and second frequencies is obvious because in order to mix two different images in fig. 9 of Kawabata-257and knowing that each image signal operates according to its* oscillator *in which the frequency is controlled by a piezoelectric crystal. Also Tanaka illustrates in fig. 3 item 7 a microcomputer. A* frequency data-mixing device for generating mixed frequency data based on each of the first and second frequencies of said first and second histogram memory devices; and *Kawabata-257in fig. 7 item 3 illustrates picture quality compensating circuit. A* compensating device for compensating the *luminance level of said input luminance signal based on said mixed frequency data", Examiner's note: Applicant uses a claim language of "a first frequency for each luminance level ..... for each predetermined period" and does not specify a value for the predetermined period. Applicant in col. 0008 discloses that the predetermined period are 1, 3, 5, 7, 5, 3, and 1 in fig. 2A. But the value of predetermined period is not clear from fig. 2A, in order a person skilled in the art selects a value (for example: 1 or 2... Second(s)).* Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Tanaka into Kawabata-257 in order to improve and the sharp variations, and remove the noise to obtain a flicker free picture.

2. Claim 2.

"The luminance level compensating apparatus according to claim 1, wherein each of said first and second histogram memory devices detects and stores said first and second frequencies for each field period, and said frequency data mixing device generates said mixed frequency data for each field period", the step of histogram memory devices is obvious because Tanaka illustrates comparison between two masking signals in different levels in Fig. 6, it means in order to be able to compare, a device should be equipped with storage area. And also Tanaka teaches in abstract that a histogram correction circuit calculates a look-up table, and a video signal correction circuit corrects the tone of the video signals using the look-up table (the LUT is stored somewhere).

3. Claim 3.

"The luminance level compensating apparatus according to claim 1, wherein said frequency data mixing device includes a multiplying device for multiplying the frequency for each luminance level stored in said first histogram memory device by a coefficient; and a selecting device for comparing the frequency for each luminance level output from said multiplying device with the frequency stored in said second histogram memory device for each luminance level and for outputting a smaller frequency of the compared frequencies as the frequency data for each luminance level of said mixed frequency data", the step is obvious because Tanaka illustrates in Fig. 4 item 17 that is (SN74ALS123) commercial advanced low-power Schottky logic. These elements equipped with different types of gates that have two inputs and one output, the two inputs multiply the data frequency in AND gate and add the two inputs in OR gate and they are equipped with small memory area. Kawabata and Tanaka do not show the detail of the frequency mixing data, for example: the multiplier, threshold, and the

accumulator. Izawa in fig. 3(b) illustrates the normalization coefficient N is multiplied to the number P of pixel in the normalization circuit 10, and the length of the ordinate is converted. a multiplier for multiplying frequency distributed data output by the first histogram memory by a frequency data coefficient; Izawa in col. 1, lines 29-55 teaches a relation between levels of the luminance signal and the number of occurrence of the levels in a predetermined time length is represented by a histogram within a predetermined range of level of the luminance signal. The data of the histogram is stored in a histogram memory, and luminance distribution on the video display is known by the data of the histogram. In the generation of the histogram data, the number of occurrence of levels in the luminance signal, which are higher than a predetermined level, is fixed to a certain constant value by a limiter circuit, and the number of occurrence of levels, which are lower than a predetermined level, is set to zero by a clip circuit. Subsequently, after addition or subtraction of a predetermined constant to or from the histogram data, cumulative addition of the histogram data is performed in the histogram cumulative addition circuit, and a cumulative histogram is obtained. A luminance level of beginning the cumulative addition and a luminance level of closing the cumulative addition in the histogram cumulative addition circuit are set in a accumulation control register circuit, and thereby a range for performing the cumulative addition of the histogram data is controlled. Izawa in fig. 2 illustrates accumulated values in the accumulators are represented by a cumulative histogram. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Izawa into Kawabata and Tanaka in order to combine the correction of the brightness level of Tanaka with Izawa as a level of an input luminance

signal for a pixel (output display) is compared with step values which change stepwise in level in a predetermined range of level, and distribution of the levels of the input luminance signal in the predetermined range of level is represented by a cumulative histogram. And also combing these options to the Kawabata invention to minimize the malfunction of the minimum brightness level for the black level compensation.

4. Claim 4.

See rejection for the claim 1, An apparatus for compensating luminance level of a signal, the apparatus comprising: a first masking circuit for masking a first predetermined image area component of a[[n]] digital video signal to output a first masked signal; a second masking circuit for masking a second predetermined image area component, which is not equal to the first predetermined image area component, of the digital video signal to output a second masked signal; a first histogram memory for storing frequency distribution data for each of a plurality of luminance levels corresponding to the first masked signal for each predetermined period; a second histogram, memory for storing frequency distribution data for each of a plurality of luminance levels corresponding to the second masked signal for each predetermined time period;

Applicant in claim 1 claims a frequency data-mixing device but in claim 4 claims the function of the frequency data-mixing device. See page 4 lines 13-20 of supplemental amendment B, by claiming a multiplier, a threshold, an accumulator and finally the compensation circuit. Kawabata and Tanaka do not show the detail of the frequency mixing data, for example: the multiplier, threshold, and the accumulator. Izawa in fig. 3(b) illustrates the normalization coefficient N is multiplied to the number P of pixel in the normalization circuit 10, and the length of the ordinate is converted. a multiplier for

multiplying frequency distributed data output by the first histogram memory by a frequency data coefficient; Izawa in col. 1, lines 29-55 teaches a relation between levels of the luminance signal and the number of occurrence of the levels in a predetermined time length is represented by a histogram within a predetermined range of level of the luminance signal. The data of the histogram is stored in a histogram memory, and luminance distribution on the video display is known by the data of the histogram. In the generation of the histogram data, the number of occurrence of levels in the luminance signal, which are higher than a predetermined level, is fixed to a certain constant value by a limiter circuit, and the number of occurrence of levels, which are lower than a predetermined level, is set to zero by a clip circuit. Subsequently, after addition or subtraction of a predetermined constant to or from the histogram data, cumulative addition of the histogram data is performed in the histogram cumulative addition circuit, and a cumulative histogram is obtained. A luminance level of beginning the cumulative addition and a luminance level of closing the cumulative addition in the histogram cumulative addition circuit are set in a accumulation control register circuit, and thereby a range for performing the cumulative addition of the histogram data is controlled.

"a minimum value selector for comparing the multiplied frequency distributed data and frequency distribution data output by the second histogram memory and for outputting smaller of the multiplied frequency distribution data and the frequency distribution data output by the second histogram memory";

Izawa in fig. 2 illustrates accumulated values in the accumulators are represented by a cumulative histogram. "an accumulator circuit for accumulating frequency distribution data output by the minimum value selector in an accumulation histogram memory";

See rejection of claim 1 for the following part of the claimed, a compensation circuit for compensating luminance level of the digital signal based on the accumulated frequency distribution data". Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Izawa into Kawabata and Tanaka in order to combine the correction of the brightness level of Tanaka with Izawa as a level of an input luminance signal for a pixel (output display) is compared with step values which change stepwise in level in a predetermined range of level, and distribution of the levels of the input luminance signal in the predetermined range of level is represented by a cumulative histogram. By combining these options to the Kawabata invention to minimize the malfunction of the minimum brightness level for the black level compensation.

5. Claim 5.

The apparatus of claim 4 further comprising an analog to digital converter for receiving an analog video signal and generating the digital signal. Izawa in fig. 1 item 2.

6. Claim 6.

The apparatus of claim 5 further comprising a synchronization separation circuit for extracting a vertical synchronizing signal and a horizontal synchronizing signal from the analog video signal and for outputting the vertical synchronizing signal and the horizontal synchronizing signal to the first masking circuit and the second masking circuit. See rejection of claims 1 and 4.

7. Claim 7.

The apparatus of claim 4, wherein said first histogram memory outputs the frequency distribution data for a first predetermined period corresponding to a horizontal scanning

period of a first number of vertical detection range lines, and said second histogram memory outputs the frequency distribution data for a second predetermined period corresponding to a horizontal scanning period of a second number of vertical detection range lines which includes the first number of vertical detection range lines. See rejection of claims 1 and 4.

8. Claim 8.

The apparatus of claim 4, wherein the compensation circuit further comprises a normalization arithmetic circuit for normalizing the accumulated frequency distribution data. Izawa in fig. 1 items 9 and 10.

9. Claim 9.

The apparatus of claim 8 further comprising a look-up table memory for storing a normalized version of the accumulated frequency distribution data. Izawa in col. 2 lines 17-22 teaches an adjustment circuit for subtracting a predetermined reference histogram value being proportional to the level of the input luminance signal from the normalized value, reference value generation means for generating a reference value which is equal to the second predetermined level of the step value generation means,

10. Claim 10.

See rejection of claim 4. A method for compensating luminance level of a digital signal, the method comprising: masking a first predetermined image area component of a digital video signal to output a first masked signal using a first masking circuit; masking a second predetermined image area component, which is not equal to the first predetermined image area component of the digital video signal, to output a second masked signal using a second masking circuit; storing frequency distribution data for

each of a plurality of luminance levels corresponding to the first masked signal for each predetermined period in a first histogram, memory area; storing second frequency distribution data for each of a plurality of luminance levels corresponding to the second masked signal for each predetermined time period in a second histogram memory area; multiplying frequency distribution data output by the first histogram memory area by a frequency data coefficient; comparing the multiplied frequency distributed data and frequency distribution data output by the second histogram, memory area; outputting smaller of the multiplied frequency distributed data and frequency distribution data output by the second histogram, memory area; accumulating frequency distribution data in an accumulation histogram memory; and compensating luminance level of the digital video signal based on the accumulated frequency distribution data.

11. Claim 11.

See rejection of claim 5. The method of claim 10 further comprising receiving an analog signal and generating the digital video signal using an analog to digital converter.

12. Claim 12.

See rejection of claim 6. The method of claim 10 further comprising extracting a vertical synchronizing signal and a horizontal synchronizing signal from the analog video signal and outputting the vertical synchronizing signal and the horizontal synchronizing signal to the first masking circuit and the second masking circuit.

13. Claim 13.

See rejection of claim 7. The method of claim 10, wherein the frequency distribution data in the first histogram memory area is output for a first predetermined period corresponding to a horizontal scanning period of a first number of vertical detection

range lines, and the frequency distribution data in the second histogram, memory area is output for a second predetermined period corresponding to a horizontal scanning period of a second number of vertical detection range lines which includes the first number of vertical detection range lines.

14. Claim 14.

See rejection of claim 8. The method of claim 10, further comprising normalizing the accumulated frequency distribution data.

15. Claim 15.

See rejection of claim 4. A system for compensating luminance level of a digital signal the system comprising: means for masking a first predetermined image area component of a digital video signal to output a first masked signal using a first masking circuit; means for masking a second predetermined image area component, which is not equal to the first predetermined image area component, of the digital video signal to output a second masked signal using a second masking circuit; a first means for storing frequency distribution data for each of a plurality of luminance levels corresponding to the first masked signal for each predetermined period; a second means for storing frequency distribution data for each of a plurality of luminance levels corresponding to the second masked signal for each predetermined period. means for multiplying frequency distribution data output by the first means for storing frequency distribution data by a frequency data coefficient; means for comparing the multiplied frequency distributed data and frequency distribution data output by the second means for storing frequency distribution data; means for outputting smaller of the multiplied frequency distributed data and frequency distribution data output by the second means for storing frequency

distribution data; means for compensating luminance level of the digital video signal based on the accumulated frequency distribution data.

16. Claim 16.

See rejection of claim 5. The system of claim 15 further comprising means for receiving an analog video signal and generating the digital video signal.

17. Claim 17.

See rejection of claim 6. The apparatus of claim 15, wherein said first means outputs the frequency distribution data for a first predetermined period corresponding to a horizontal scanning period of a first number of vertical detection range lines, and said second means outputs the frequency distribution data for a second predetermined period corresponding to a horizontal scanning period of a second number of vertical detection range lines which includes the first number of vertical detection range lines.

18. Claim 18.

See rejection of claim 8. The system of claim 15 further comprising means for normalizing the accumulated frequency distribution data.

19. Claim 19.

See rejection of claim 9. The system of claim 18 further comprising means for storing a normalized version of the accumulated frequency distribution data.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Javid A Amini
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